REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested in view of the above amendments and the following remarks.

Claims 1, 2, 4, 5, and 7-15 are pending in this application. By this amendment, Claims 1-6 and 8-15 have been amended. Support for the amendments to Claims 1 and 13 is found, by way of non-limiting example, in canceled Claims 3 and 6, and the specification page 17, lines 3-16. Accordingly, it is respectfully submitted that no new matter has been added.

Claim 10 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants acknowledge with appreciation the indication that Claim 10 includes allowable subject matter, however, because Applicants consider that Claims 1 and 13 amended to incorporate the subject matter of canceled Claims 3 and 6 distinguishes from the cited references, Claim 10 has been presently maintained in dependent form.

As the amendments to Claims 1 and 13 incorporate the essential subject matter of canceled Claims 3 and 6, it is respectfully submitted that this amendment does not raise new issues requiring further consideration and/or search. Accordingly, it is respectfully requested that this amendment be entered as a matter of right.

In the outstanding Office Action, Claim 3 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite; Claims 1-3, 7, 9, 11, and 13-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stroud et al. (Applying Built-in Self-Test to Majority Voting Fault Tolerant Circuits, IEEE 1998, hereinafter "Stroud") in view of Butts et al. (U.S. 5,036,473, hereinafter "Butts"); Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Stroud in view of Butts and further in view of Kraus et al. (U.S. Patent No.

6,587,979 B1, hereinafter "Kraus"); Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Stroud in view of Butts and further in view of Baeg et al. (U.S. Patent No. 5,805,608, hereinafter "Baeg"); Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Stroud in view of Butts and further in view of Lai et al. (U.S. Patent No. 6,691,079 B1, hereinafter "Lai"); and Claims 8 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stroud in view of Butts and further in view of Gaubatz (U.S. Patent No. 5,621,776).

Applicants hereby express appreciation for the grant of a personal interview on March 30, 2010. During the interview, arguments were made consistent with the remarks to follow that the amended claims are patentable over the cited references. In response to the discussion during the interview the language of Claims 6 as added to independent Claims 1 and 13 has been modified to delete "or determining whether the number of the input patterns is sufficient" and to recite that "whether the output logic patterns corresponding to the input logic patterns coincide with predicted patterns calculated from design specifications to verify that the functional units are correctly connected to each other." This language is consistent with the language in the specification page 17, lines 3-16.

The rejection of Claim 3 under 35 U.S.C. § 112, second paragraph, is respectfully traversed. In the safety protection instrumentation system recited in previous Claim 1, the digital logic includes a plurality of functional units having logic circuitry in which output logic patterns corresponding to all potential input logic have been verified in advance and a functional module formed by combining the plurality of functional units so as to form a logic structure different from the logic structure of each of the plurality of functional units individually.

In other words, a small functional unit or element (soft) is output in a different FPGA in advance and, subsequently, logic is verified by a circuitry (hard) on that FPGA.

Thereafter, by using the verified plural functional units, plural combinations thereof constitute the entire functional module (soft) to thereby install into another FPGA unit (element) different from the verified FPGA to constitute the circuitry (hard).

On the other hand, the safety protection instrumentation system of Claim 3 represents a structure confirming, on the soft, that the logic constitution (soft) in the functional units is not different from the logic constitution of the verified time at the time of making the entire functional module (soft), the plural combination using a plurality of functional units recited in previous Claim 1.

Claim 1 has been amended by incorporating the subject features of the current Claims 3 and 6 into the Claim. A similar amendment has been made to Claim 13.

The assertion in the Office Action that the function verification of FPGA by toggle coverage of Claim 6 is a known matter may be correct. However, in the present invention, as recited in amended Claims 1 and 13, when the functional module of the entirety is formed by combining the plurality of functional units, the toggle coverage is verified only with respect to the connection between the functional units. The toggle coverage sets a certain inspection objective coverage, and within this coverage, the toggle coverage is verified with the number of signals being parameter and the number of signals changed by test pattern.

Thus, the present invention as recited in Claims 1 and 13 differs in that the inspection objective coverage only selects the connection between the functional units. (In actuality, the signal in the functional unit is removed from the inspection objective coverage and the other signals are considered to be connection between functional units.)

That is, the present invention as recited in amended Claims 1 and 13 is characterized in that when the software logic of the functional units are verified by installing individually in the FPGA and then verified through the verification original test (Claim 1), it is confirmed that the software formed by combining the recited elements thus does not change in the logic

structure in the functions in the functional units (previous Claim 3), and then, the functions in the functional units have the same performance as in the inspection test. Therefore the toggle coverage verifies that the connection between the functional units are not incorrect (previous Claim 6). Therefore, Claims 1 and 13 recite that the invention determines whether the output logic patterns corresponding to the input logic patterns coincide with predicted patterns calculated from design specifications to verify that the functional units are correctly connected to each other as described in the specification page 17, lines 3-16.

According to such an apparatus and process as recited in Claims 1 and 13, respectively, it is confirmed that the entire soft logic is correctly operated.

Kraus, Baeg, Lai, Gaubatz and Dennis fail to correct the deficiencies of Stroud above because neither of these references describes the features of Claims 1 and 13 quoted above.

Accordingly, it is respectfully requested that the rejections of Claims 1-15 be reconsidered and withdrawn, and that Claims 1, 2, 4, 5 and 7-15 be found allowable.

Consequently, for the reasons discussed in detail above, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. Therefore, a Notice of Allowance is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact the undersigned representative at the below-listed telephone number.

Respectfully submitted,

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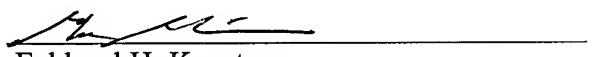

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